IN THE CLAIMS

1. (Original) A memory device comprising:

a plurality of banks, each including a plurality of memory cores;

a plurality of sense amplifiers shared among memory cores of different ones of the plurality of banks; and

wherein the memory cores from two of the different ones of the plurality of banks are interleaved in a strip with the plurality of shared sense amplifiers.

2. (Currently Amended) The memory device of claim 1 wherein the ~~strip is arranged in a row, and~~ column decode conductors traverse the memory cores in the strip.

3. (Original) The memory device of claim 2 further comprising sense nodes substantially parallel to the column decode conductors.

4. (Original) The memory device of claim 1 wherein the plurality of memory cores are arranged into a plurality of strips, each strip including interleaved memory cores from two different ones of the plurality of banks.

5. (Currently Amended) A memory device comprising:

a plurality of memory cores logically arranged into a plurality of banks;

a plurality of sense amplifiers shared among memory cores of two of the plurality of banks; and

wherein the memory cores of the two of the plurality of banks are ~~interleaved in a~~ arranged in a strip in an alternating fashion of banks between ones of the plurality of sense amplifiers. ~~row~~.

6. (Currently Amended) The memory device of claim 5 further comprising column decode conductors for the strip ~~row~~, the column decode conductors for the strip ~~row~~ being coupled to the plurality of sense amplifiers shared among the memory cores of the two of the plurality of banks.

7. (Currently Amended) The memory device of claim 5 ~~6~~ wherein the plurality of memory cores are arranged in a plurality of first strips which correspond to the strip ~~rows~~ and a plurality of second strips arranged perpendicular to the first strips, ~~columns,~~ each of the plurality of first strips ~~rows~~ including interleaved memory cores from two different ones of the plurality of banks.

8. (Currently Amended) The memory device of claim 5 wherein the plurality of memory cores are arranged in a plurality of first strips ~~rows~~ and a plurality of second strips arranged perpendicular to the first strips ~~columns~~, each of the plurality of first strips ~~rows~~ including interleaved memory cores from two different ones of the plurality of banks.

9. (Currently Amended) A memory device comprising:

a first bank of memory cores arranged in a linear strip;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the linear strip; and

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank along the linear strip.

10. (Currently Amended) The memory device of claim 9 further comprising a plurality of memory cores arranged as horizontal strips ~~rows~~ and a plurality of memory cores of vertical strips arranged perpendicular to the horizontal strips ~~columns~~, wherein the linear strip is one of the plurality of horizontal strips ~~rows~~.

11. (Currently Amended) The memory device of claim 10 wherein each of the plurality of horizontal strips ~~rows~~ includes interleaved memory cores from two different banks.

12. (Original) The memory device of claim 9 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

13. (Cancel)

14. (Original) A memory device comprising:

a first bank of memory cores arranged in a strip;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip;

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank; and

a column decoder arranged to drive column decode lines coupled to the plurality of sense amplifiers.

15. (Currently Amended) The memory device of claim 14 further comprising a plurality of memory cores arranged in horizontal strips ~~rows~~ and a plurality of memory cores arranged in vertical strips arranged perpendicular to the horizontal strips ~~columns~~, wherein the strip is one of the plurality of horizontal strips ~~rows~~.

16. (Currently Amended) The memory device of claim 15 wherein each of the plurality of horizontal strips ~~rows~~ includes interleaved memory cores from two different banks.

17. (Original) The memory device of claim 14 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

18. (Currently Amended) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension; and

wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank interspersed with shared sense amplifiers between memory cores of different banks.

19. (Currently Amended) The integrated circuit of claim 18 wherein the first dimension includes a plurality of horizontal strips ~~rows~~ of memory cores, and the second dimension includes a plurality of vertical strips ~~columns~~ of memory cores, and each of the plurality of horizontal strips ~~rows~~ includes interleaved memory cores from two different banks.

20. (Currently Amended) The integrated circuit of claim 19 wherein each of the plurality of vertical strips ~~columns~~ includes non-interleaved memory cores from different banks.

21. (Original) The integrated circuit of claim 18 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder and situated substantially parallel to the strip of memory cores.

22. (Original) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank; and

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank.

23. (Currently Amended) The integrated circuit of claim 22 wherein:

the first dimension includes a plurality of horizontal strips ~~rows~~ of memory cores;

the second dimension includes a plurality of vertical strips ~~columns~~ of memory cores; and

each of the plurality of horizontal strips ~~rows~~ includes interleaved memory cores from two different banks.

24. (Currently Amended) The integrated circuit of claim 23 wherein each of the plurality of vertical strips ~~columns~~ includes non-interleaved memory cores from different banks.

25. (Original) The integrated circuit of claim 22 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder, coupled to the plurality of sense amplifiers, and situated substantially parallel to the strip of memory cores.

26. (Original) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank;

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank; and

column decode conductors coupled to the plurality of sense amplifiers, the column decode conductors arranged to be near memory cores of the first and second bank, and not near memory cores of other banks.

27. (Currently Amended) The integrated circuit of claim 26 wherein the first dimension includes a plurality of horizontal strips ~~rows~~ of memory cores, and the second dimension includes a plurality of vertical strips ~~columns~~ of memory cores, and each of the plurality of horizontal strips ~~rows~~ includes interleaved memory cores from two different banks.

28. (Currently Amended) The integrated circuit of claim 27 wherein each of the plurality of vertical strips ~~columns~~ includes non-interleaved memory cores from different banks.

29. (Currently Amended) A memory device comprising:

a first bank of memory cores;

a second bank of memory cores; and

a plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores;

wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first horizontal strip ~~row~~ on the memory device.

30. (Currently Amended) The memory device of claim 29 further comprising:

a plurality of horizontal strips ~~rows~~ of which the first horizontal strip ~~row~~ is one; and

a plurality of vertical strips ~~columns~~ of memory cores, each of the plurality of vertical strips ~~columns~~ of memory cores having non-interleaved memory cores from a plurality of banks.

31. (Currently Amended) The memory device of claim 29 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second horizontal strip ~~row~~ parallel to the first horizontal strip ~~row~~.

32. (Original) The memory device of claim 29 further comprising pass transistors coupled to the plurality of sense amplifiers to select data from either the first bank of memory cores or the second bank of memory cores.

33. (Currently Amended) A memory device comprising:

a first bank of memory cores;

a second bank of memory cores, wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first horizontal strip ~~rows~~ on the memory device;

a plurality of sense amplifiers shared between the first bank of cores and the second bank of cores;

a column decoder; and

a plurality of column decode conductors coupled to the column decoder and the plurality of sense amplifiers, the plurality of column decode conductors being substantially parallel to the first horizontal strip ~~row~~ on the memory device.

34. (Currently Amended) The memory device of claim 33 further comprising:

a plurality of horizontal strips ~~rows~~ of which the first horizontal strip ~~row~~ is one; and

a plurality of vertical strips ~~columns~~ of memory cores, each of the plurality of vertical strips ~~columns~~ of memory cores having non-interleaved memory cores from a plurality of banks.

35. (Currently Amended) The memory device of claim 33 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second horizontal strip ~~row~~ parallel to the first horizontal strip ~~row~~.

36. (Currently Amended) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips ~~rows~~ and vertical strips ~~columns~~ and logically arranged into banks that share sense amplifiers, wherein memory cores arranged in a first horizontal strip ~~row~~ alternate between a first bank and a second bank.

37. (Original) The memory device of claim 36 further comprising:

a column decoder;

column decode conductors coupled between the column decoder and the sense amplifiers shared between the first bank and the second bank; and

sense nodes coupled to the sense amplifiers, arranged substantially parallel to the column decode conductors.

38. (Currently Amended) The memory device of claim 36 wherein memory cores in a second horizontal strip ~~row~~ are arranged to alternate between a third bank and a fourth bank.

39. (Currently Amended) The integrated circuit of claim 36 wherein each of the of vertical strips ~~columns~~ includes non-interleaved memory cores from different banks.

40. (Currently Amended) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips ~~rows~~ and vertical strips ~~columns~~ and logically arranged into banks that share sense amplifiers, wherein memory cores arranged in a first horizontal strips ~~row~~ alternate between a first bank and a second bank; and

column decode conductors arranged in the first horizontal strip ~~row~~ to cross memory cores from the first bank and the second bank.

41. (Currently Amended) The memory device of claim 40 further comprising:

a second horizontal strip ~~row~~ having interleaved memory cores from a third bank and a fourth bank; and

a second plurality of sense amplifiers shared between the third bank and the fourth bank.

42. (Currently Amended) The memory device of claim 40 wherein each of the vertical strips ~~columns~~ includes non-interleaved memory cores from different banks.

43. (Currently Amended) A memory device comprising:

a plurality of memory cores physically arranged in a plurality of horizontal strips ~~rows~~ and a plurality of vertical strips ~~columns~~ and logically arranged into banks;

wherein memory cores arranged in each of the plurality of horizontal strips ~~rows~~ alternate between two banks, and memory cores arranged in each of the plurality of vertical strips ~~columns~~ are from a different bank.

44. (Currently Amended) The memory device of claim 43 further comprising sense amplifiers shared between memory cores in each of the plurality of horizontal strips ~~rows~~.

45. (Currently Amended) The memory device of claim 44 further comprising column decode conductors dedicated to each horizontal strip ~~row~~, each column decoder conductor passing over memory cores of two banks and no more.

46. (Currently Amended) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a plurality of horizontal strips ~~rows~~ and vertical strips ~~columns~~ of memory cores; and

a plurality of sense amplifiers positioned between memory cores within each horizontal strip ~~row~~, wherein every other memory core within each horizontal strip ~~row~~ is assigned to a bank.

47. (Original) The computer system of claim 46 wherein each sense amplifier is shared between two banks.

48. (Original) The computer system of claim 46 further comprising a memory controller coupled to the processor and the memory device.

49. (Currently Amended) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a first bank of memory cores arranged in a first horizontal strip ~~row~~;

a second bank of memory cores interleaved with the first bank of memory cores in the first horizontal strip ~~row~~;

a third bank of memory cores arranged in a second horizontal strip ~~row~~; and

a fourth bank of memory cores interleaved with the third bank of memory cores in the second horizontal strip ~~row~~.

50. (Original) The computer system of claim 49 wherein the memory device further includes:

a first plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores; and

a second plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores.

51. (Original) The computer system of claim 49 further comprising a memory controller coupled to the processor and the memory device.

52. (Original) A computer system comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of sense amplifiers;

a first bank of memory cores, each coupled to at least one of the plurality of sense amplifiers; and

a second bank of memory cores, each coupled to at least one of the plurality of sense amplifiers;

wherein the first bank of memory cores and the second bank of memory cores are arranged in a strip with the plurality of sense amplifiers.

53. (Original) The computer system of claim 52 wherein the memory further includes:

column decode conductors coupled to the plurality of sense amplifiers and

a column decoder to drive the column decode conductors.

54. (Original) The computer system of claim 52 further comprising a memory controller coupled to the processor and the memory device.

55. (Currently Amended) A computer system comprising:

a processor;

a memory controller coupled to the processor; and

a memory device coupled to the memory controller, the memory device including:

a plurality of memory cores logically arranged into Rambus-compatible banks and physically arranged into horizontal strips ~~rows~~ and vertical strips ~~columns~~, wherein each vertical strip ~~column~~ includes interleaved memory cores from two different Rambus-compatible banks.

56. (Currently Amended) The computer system of claim 55 wherein the memory device includes sense amplifiers shared between memory cores of Rambus-compatible banks in each horizontal strip ~~row~~.

57. (Currently Amended) A multibank memory device allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:

a plurality of memory banks, each memory bank including a plurality of memory cores arranged in strips of horizontal strips ~~rows~~ and vertical strips ~~columns~~;

a plurality of sense amplifiers shared among the memory cores of different ones of the plurality of memory banks;

a plurality of column decoders, each column decoder exclusively accessing a horizontal strip ~~row~~ of memory cores from only two of the plurality of memory banks wherein the memory cores are separated from each other in the horizontal strip by shared sense amplifiers whereby the memory cores of the horizontal strip alternate between the two memory banks.

58. (Currently Amended) A memory architecture having n banks of memory banks which allows simultaneous access of some of the memory banks, comprising a plurality of memory banks, each memory bank including a plurality of memory cores arranged in horizontal strips ~~rows~~, each horizontal strip ~~row~~ having an associated column decoder connected to each memory core of the horizontal strip ~~row~~ and each core of the horizontal strip ~~row~~ associated with only one of two memory banks.

59. (Previously Presented) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:

a plurality of memory banks, each memory bank containing a plurality of memory cores arranged in strips, each strip containing two memory banks and the strip having cores arranged to be alternating between the two memory banks with sense amplifiers shared between the cores of the two memory banks.

60. (Currently Amended) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks comprising a horizontal strip ~~row~~ of memory cores interspersed between shared sense amplifiers, each memory core being a part of one of N memory banks, the strip having the memory cores laid out so that no two memory cores of the same memory bank share a common sense amplifier.

REMARKS

Applicant has carefully reviewed and considered the Final Office Action mailed on March 20, 2003, and the Advisory Action mailed June 17, 2003, and the references cited therewith. In response thereto, Applicant submits the following remarks in support of patentability with amendment to claims.

In this amendment, claim 13 is deleted and claims 2, 4-11, 15, 16, 18-20, 23-24, 27-31, 33-36, 38-46, 38-46, 49 and 55-60 have been amended. Thus claims 1-12 and 14-60 remain pending in the present patent application. Reconsideration of the claims, removal of the rejections and allowance of all claims is respectfully solicited.

Interview Summary

Applicant thanks Examiner Trong Phan for the courtesy of a telephone interview on July 23, 2003. In the interview, Applicant's representative explained what is believed to be the source of confusion regarding the drawing in Figure 3. Applicant explained that the use of the words "row" and "column" were only used to reference directions in Figures 1 and 3, not to describe internal rows and columns of memory bank operations. The specification describes Figures 1 and 3 in terms of rows (or strips) and columns. This is because the layouts shown in these figures lend themselves to such a description. A column in a drawing is a vertical structure, such as the columns on the Greek Parthenon. A row is a horizontal structure such as the rows of seats at a ballgame. The use of row and column descriptors used to describe Figures 1 and 3 has nothing to do with the words row and column found inside the DRAM memory banks of Figure 1 and 3.

The Examiner indicated that Applicant should amend the claims to remove the words "row" and "column" so as to avoid confusion. Although a patent drafter is allowed to be his or her own lexographer, Applicant agreed to amend the claims to avoid the confusion.

In the Drawings

The drawings were objected to under 37 C.F.R. 1.83(a) since the drawings allegedly did not show every feature of the invention specified in the claims. The feature of the memory cores from two of the different ones of the plurality banks are interleaved in a strip with the plurality of shared

sense amplifiers as recited in claims 1-60 and their connective relationship is alleged to be missing. Since the claims have now been amended to remove the words "rows" and "columns" there is no need to amend the drawings.

§112 Rejection of the Claims

Claims 1-60 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses this rejection since the claimed interleaving connective relationship between the memory cores is already shown in Figure 3. Since the claims have now been amended to remove the words "rows" and "columns" this rejection is obviated.

§103 Rejection of the Claims

Claims 1-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa (U.S. 5,970,016) in view of Morton (U.S. 5,159,572). Applicant respectfully traverses this rejection on several grounds described below. For the reasons stated above in the interview summary, Applicant has deemed that the claims do not require further amendment since they already distinguish over the art of record.

The Ohsawa patent describes a DRAM device with memory banks capable of independent operation, such as Rambus and the like. (Ohsawa, col. 1, lines 7). This architecture is similar to the architecture shown in Applicant's patent application in conjunction with Figure 1. As a result of this architecture, the Ohsawa patent suffers from the same noise problems in Multi-bank operation as described by Applicant in conjunction with Figure 1. However, Ohsawa does not recognize the problem or provide a solution for the sense amplifier noise resulting from adjacent column decode lines being active at the same time during simultaneous multi-bank operation.

The Morton patent describes a very old DRAM architecture which uses distributed row address decode and uses interleaved word line signals in a cell array. For example, Figure 3 of the Morton patent shows cell array 26 having rows of cells being address from both word line decode units 48 and 48' (see arrows alternating in left and right directions). This use of the term

"interleaving" refers only to local word lines and has nothing to do with alternating banks of memory. Further, the Morton patent describes a traditional DRAM from approximately 13 years ago that was not capable of simultaneous access of multiple banks of memory such as the type found in the Ohsawa patent. Hence, the Morton patent fails to teach an interleaving of different ones of a plurality of banks in a strip with shared sense amplifiers. Morton also fails to describe sense amplifiers which are shared between banks of memory (there are no banks of memory in Morton). Morton and Ohsawa also fail to even identify any noise problems in sense amplifiers associated with multiple memory bank access.

Since all of the elements of the claimed invention are not found in the combination of references cited in the First Office Action, the rejection of claims 1-60 under 35 U.S.C. §103(a) must fail. Applicant respectfully requests reconsideration of the claims and allowance of all claims.

Examiner's Response to Applicant's Arguments

In the Advisory Action, the Examiner gave two interpretations of how the present invention is connected. As described above, the use of the words row and column in the claims were never intended to discuss intra-memory bank interconnections, but rather meant only to describe relative directions. Now that the terms "rows" and "columns" have been removed from the claims, Applicant respectfully requests that the Examiner focus on the inter-bank structure of the present invention, which provides great advantages in DRAM design.

In the previous office action, the Examiner has treated all 60 claims as a single group in the rejections. All 60 claims contain different limitations, contain many different independent claims and cannot be judged as a group. Therefore, Applicant respectfully requests that the individual claims be examined and the limitations of each claim be taken into account and compared to the prior art if any further rejections are forthcoming.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 612-373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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